VELSANET

Structure-Native Network Architecture

White Paper #23

6G RU: Multi-User Physical Mapping Design

— Structure-Native Physical Path Direct Mapping (No-Switching) —

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1. Hardware-Based Multi-Access Mechanism

This design eliminates software schedulers entirely. All multi-user signals are mapped to optical cores in real time through dedicated hardware logic — not through OS-level arbitration or packet queuing. The physical structure of the RU is the network.

1.1 Spatial Multiplexing and Slot Assignment (Spatial → Slot)

- **8-Channel MIMO:** Signals from multiple users collected at the antenna layer are spatially separated, producing 8 independent wireless streams. Each stream represents a distinct spatial direction — not a distinct user identity.
- **Time-Sensitive Gearbox:** The 8 separated wireless data streams are fixed-mapped 1:1 onto 8 Physical Slots within a single optical core. No buffering occurs. No wait state exists. The mapping is deterministic and immediate.

> *Design principle: The Time-Sensitive Gearbox is not a scheduler. It is a fixed hardware interconnect that aligns wireless stream timing to optical slot timing. Once a stream enters a slot, it exits the other end of the fiber at the speed of light with no intermediate logic.*

1.2 Sector-to-Core Physical Direct Link

- **Fixed Interconnect:** The Coherent Optical Engine inside the RU is physically wired to transmit data from a specific sector exclusively onto a designated core (Core #N) within the 48-core MOCT ribbon. This wiring is established at manufacture — not configured at runtime.

- **Structure-Native:** The system does not compute who the user is. It routes data based solely on which sector the signal arrived from, onto a pre-assigned dedicated optical path. Identity is irrelevant; direction is everything.

"Physical infrastructure is the network's logical structure."

This is the foundational departure from conventional RAN design. Legacy systems identify users, schedule transmissions, manage sessions, and arbitrate across shared resources. In Velsanet Structure-Native RAN, none of these operations exist. The physical path is the only logic.

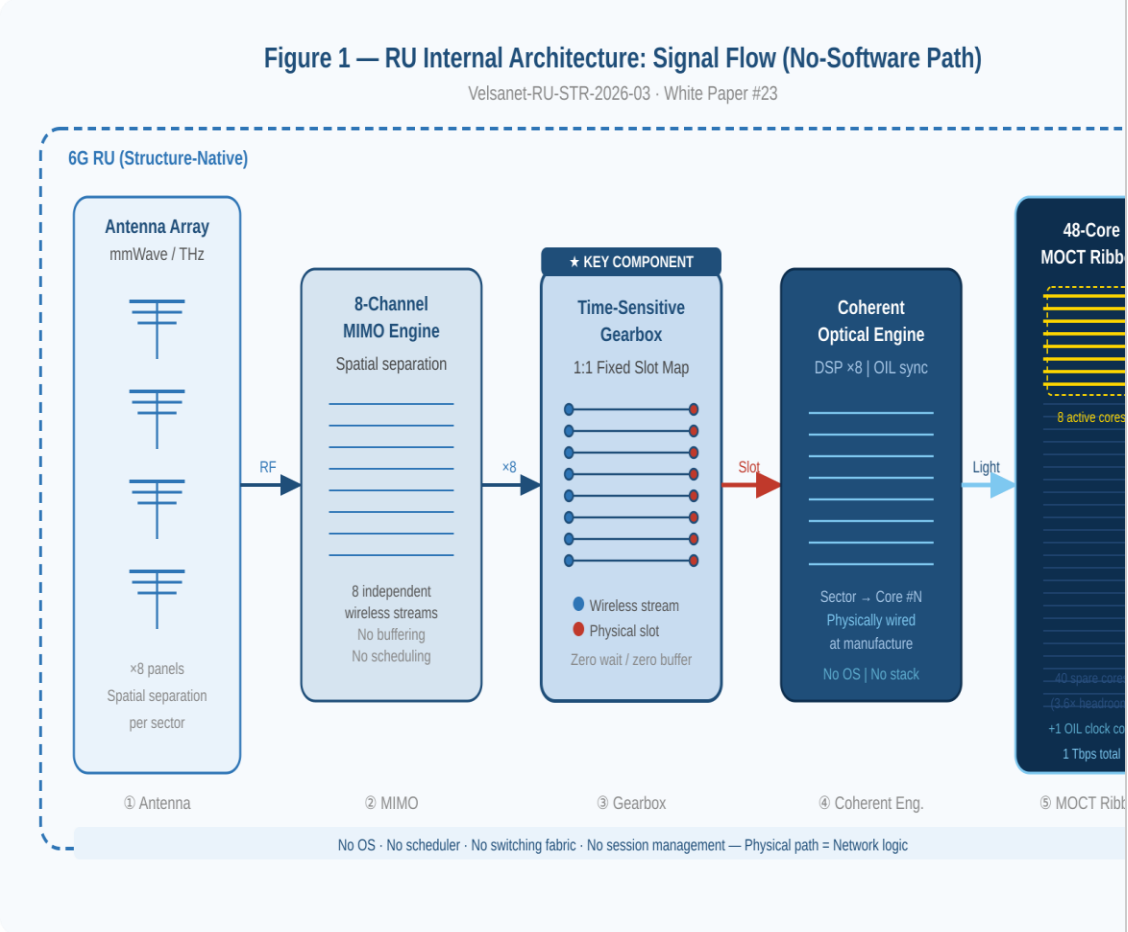

Figure 1 — RU Internal Architecture: Antenna → MIMO → Time-Sensitive Gearbox → Coherent Optical Engine → 48-Core MOCT Ribbon

2. Capacity and Scalability Design

Category	Design Specification	Note
Base Capacity	1 Tbps / core (8-channel	*High-density user absorption per single core*

	aggregate)	
Structural Headroom	48-Core MOCT Ribbon	*3.6× core surplus vs. subscriber count*
Dynamic Expansion	Spare Core Activation	*Physical path extension on traffic surge*
Synchronization	Optical Injection Locking	*Physical alignment of all user signals*

The 48-core MOCT ribbon provides a structural surplus ratio of 3.6× over Seoul's 12 million mobile subscriptions. This surplus is not waste — it is the physical substrate for future demand: IoT sensors, V2X channels, high-density video, and PAI-native machine coordination. When capacity is needed, spare cores are activated. No new civil works. No software reconfiguration. Physical paths are added.

> *Optical Injection Locking allocates 1 of 48 cores exclusively to clock distribution. H6 transmits the reference clock to RU via optical carrier. The RU's Coherent Optical Engine locks onto this signal and synchronizes all 8 DSP channels. Clock jitter is eliminated by physical propagation — not by packet-based correction algorithms.*

3. Elements Structurally Eliminated

The following table summarizes the layers and mechanisms that conventional RAN architectures require and that Velsanet Structure-Native RAN does not implement. Elimination is architectural — not a configuration option.

Eliminated Element	Legacy Approach	Velsanet Structure-Native
Software Scheduler	OS-level packet scheduling, queuing, priority arbitration	Eliminated — hardware-fixed sector-to-core mapping
Switching Fabric	Electronic crossbar / forwarding table lookup	Eliminated — physical ribbon core pre-assigned at manufacture
DU / CU Stack	Virtualized distributed/centralized unit software	Eliminated — structural path replaces logical layer
Session Management	User identity computation, authentication per handover	Eliminated — direction-based physical routing, no identity check
Clock Distribution	PTP / IEEE 1588 packet-based clock recovery	Eliminated — Optical Injection Locking via dedicated core

The consequence of this elimination is absolute: no OS boot, no software fault surface, no scheduler latency, no session re-establishment on handover. The RU has no software state. It is a precision optical-wireless transducer — and nothing more.

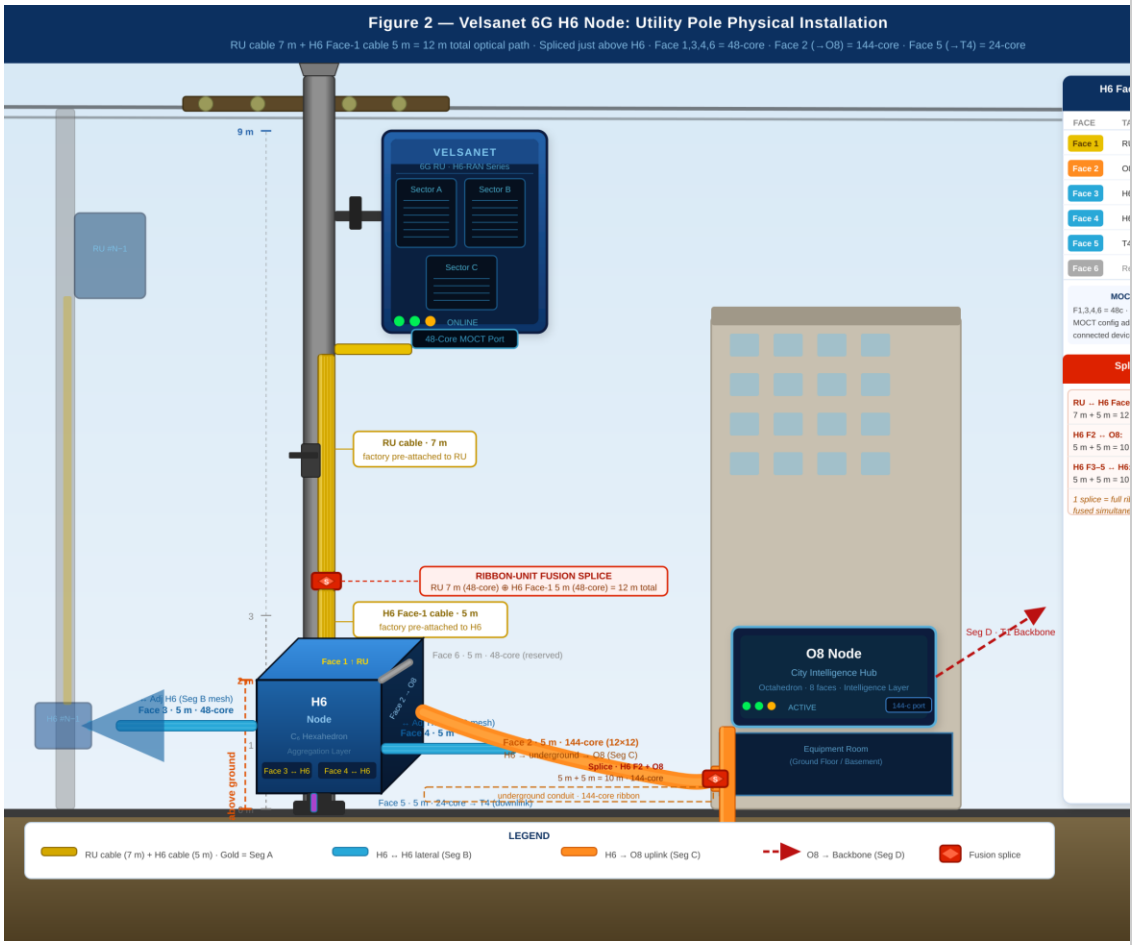

Figure 2 — Velsanet 6G RU: Utility Pole Physical Installation (Seoul Metropolitan, ~400,000 poles)

4. Architectural Significance

Conventional 6G targets define extreme performance as a specification to be achieved by sophisticated software. Velsanet inverts this: extreme performance is the natural output of structural simplicity. By removing every software layer between antenna and optical core, the RU achieves 6G's 1 Tbps target and sub-millisecond latency as emergent properties of its physical geometry.

This design is not an optimization of legacy RAN. It is a different class of device. The 900,000 RUs deployed across Seoul's 400,000 utility poles are not base stations with software stacks — they are physical transducers in a city-scale optical mesh. When the mesh is complete, Seoul's infrastructure will be the first instance of what may properly be called:

A Physical Intelligence Grid — the first of its kind.

Each RU contributes one node to this grid: a fixed optical path from a physical direction in space to a defined core in a ribbon cable. Multiply that by 900,000 nodes, 48 cores each, across 785,690 km of optical infrastructure — and the result is not a

network. It is a structured physical medium for intelligence.

5. Hardware Block Detailed Design Specification

This section defines the internal hardware architecture of the Velsanet 6G RU at the block level. Three functional blocks constitute the complete signal path from antenna to optical core: the Time-Sensitive Gearbox (TSG), the 48-Core MOCT Physical Interface, and the Optical Injection Locking (OIL) synchronization unit. Together they form a zero-software, hardware-native transduction chain.

5.1 Time-Sensitive Gearbox (TSG) — Core Mapping Logic

Function

Velsanet's design responsibility begins at the TSG input. RF processing — antenna, beam-forming, PHY, MAC, A/D conversion — is performed by the 6G RU and is outside Velsanet scope. The TSG receives 8-channel parallel digital baseband output from the 6G RU and performs a strictly 1:1 fixed mapping to 8 assigned optical slots. It contains no scheduling logic, no priority queue, no buffer management, and no software interrupt path. It operates as a pure hardware interconnect: signals enter at the RF/optical boundary and exit into the Coherent Optical Engine without any intermediate state.

Implementation

The TSG is implemented as a fixed-delay wiring fabric within a dedicated FPGA or custom ASIC. Each of the 8 input channels is hard-wired to a corresponding output lane through nanosecond-precision delay lines. The delay is matched across all 8 channels to within ±50 ps to ensure slot alignment at the optical engine input. There is no clock domain crossing logic, no FIFO, and no reconfigurable routing plane. The mapping is physically determined at manufacture and cannot be altered in the field.

Internally, the FPGA fabric contains 8 independent parallel signal paths, each with a fixed propagation delay of less than 2 ns end-to-end. No time-division multiplexing occurs within the TSG: each channel occupies its dedicated physical path at all times.

Differentiation from Legacy RAN

Legacy RAN architectures employ OS-based packet queuing at the DU layer, introducing variable latency of 0.1–10 ms depending on scheduler load. The TSG eliminates this regime by replacing the scheduler with physical slot alignment. The latency contribution of the TSG is bounded by its fixed propagation delay — approximately 2–5 ns, versus 100,000–10,000,000 ns in software-scheduled systems.

5.2 48-Core MOCT Physical Interface

Physical Configuration

The MOCT interface consists of 48 single-mode optical fiber cores in a flat ribbon geometry. Core assignments are permanent and functionally differentiated:

Core #1 — Channel 1 (structural sensing and control). Device authentication, physical alignment verification, and self-awareness bootstrap per WP#03 and WP#20. Carries no user data.

Core #48 — Clock reference core (Optical Injection Locking). Carries a continuous-wave optical reference signal from H6 to RU. Carries no user data. See Section 5.3.

Cores #2–#47 — 46 active data cores. Each core is hard-wired to a specific sector signal output from the Coherent Optical Engine. The mapping is physically determined at manufacture.

Hard-Wired Sector-to-Core Assignment

The Coherent Optical Engine is physically wired such that each sector's optical output feeds exclusively into its pre-designated core. Sector A occupies Core #2–#17 (16 cores). Sector B occupies Core #18–#33. Sector C occupies Core #34–#47. This distribution is fixed in the photonic substrate at manufacture.

Structural Headroom: 3.6x Capacity Reserve

Against Seoul's subscriber density baseline, the 46 active data cores provide 3.6x the physical capacity required at peak load. When traffic demand increases, idle cores are activated by the optical engine without any software reconfiguration — no provisioning cycle, no software update, no network re-convergence.

5.3 Optical Injection Locking (OIL) — Physical Synchronization Unit

The Synchronization Problem in Conventional RAN

Conventional RAN synchronization relies on IEEE 1588 PTP or GPS-derived timing transmitted as packet payloads across IP/Ethernet networks. Because packets traverse queues, the timing signal is subject to variable latency from path asymmetry, queuing delay, and processing jitter. Residual clock jitter is typically 10–100 ns, with worst-case excursions exceeding 1 µs under congestion. This jitter propagates directly into 6G modulation timing.

Operating Principle

OIL replaces the packet-based timing signal with a continuous-wave (CW) optical reference signal transmitted over Core #48. The H6 node emits a spectrally pure CW laser signal into Core #48. At the RU, the Coherent Optical Engine contains a slave laser whose cavity is optically coupled to Core #48. The slave laser undergoes injection locking: its oscillation frequency and phase are captured by the incoming reference wave, synchronizing the RU's optical engine to the H6 clock source at the physical level. No packet is transmitted. No timestamp is parsed. No algorithm computes a correction offset. The lock is established and maintained by the physics of optical resonance — specifically, the Adler equation governing injection locking bandwidth.

Synchronization Precision

Once injection lock is established, the RU slave laser maintains phase coherence with the H6 reference to within femtosecond (10^-15 s) accuracy — four to five orders of magnitude better than packet-based PTP. The jitter of the synchronized clock is bounded only by the phase noise floor of the H6 master laser and the shot noise of the optical path, both deterministic physical constants.

Lock Acquisition Sequence

The OIL acquisition sequence proceeds entirely in hardware:

Step 1 — H6 powers on. Core #48 CW reference signal begins propagating immediately.

Step 2 — RU powers on. Slave laser detects CW signal on Core #48 within nanoseconds of first photon arrival.

Step 3 — Injection locking engages. Lock acquisition time is approximately 1–10 µs.

Step 4 — Lock confirmed. RU optical engine transmits structural identity signal via Core #1 Channel 1 to H6. Self-awareness bootstrap completes per WP#20.

Step 5 — Data cores (Core #2–#47) activate. RU enters operational state. Total boot time under 100 ms, with no software initialization path.

Velsanet Clock Hierarchy

The OIL architecture extends vertically through the full Velsanet hierarchy: I20 → D12 → O8 → H6 → RU. The root clock source resides at the I20 tier, where a GPS-disciplined or atomic reference laser serves as the ultimate frequency standard. Each tier locks optically to its parent. No packet crosses the clock path at any level. The entire clock tree is a passive optical phenomenon propagating deterministically through fixed physical paths.

Environmental Stability

Thermal variation in the ribbon cable causes minor changes in fiber refractive index. Single-mode silica fiber exhibits a thermo-optic coefficient of approximately 10^-5 /K, producing a phase shift of 0.1 rad/K over a 7 m path. The MOCT MEMS alignment layer (WP#03 Section 8.3) compensates for thermally induced mechanical displacement. Residual phase drift is absorbed within the injection locking bandwidth of the slave laser cavity (designed to exceed 1 GHz), making sub-Hz thermal drift negligible. Clock stability is maintained across -20°C to +60°C without active compensation circuitry.

6. Bill of Materials (BOM)

This section defines the complete material composition of the Velsanet 6G RU at the unit level. The BOM is organized into two sub-levels: RU internal components, and pole-site assembly including inter-node cabling. All ribbon cables are factory pre-attached and shipped as integral extensions of their respective nodes.

6.1 6G RU Internal BOM (per unit)

#	Assembly / Block	Component / Specification	Key Parameter	Qty	
	RF Interface Requirements (6G RU Manufacturer Scope)				
1	**RF Output Interface**	8-channel MIMO output from 6G RU — per manufacturer spec (sub-THz/ mmWave). Velsanet defines the interface requirement only; antenna design is outside Velsanet scope.	8 independent RF output channels, sector-aligned	Per RU mfr.	
2	**TSG Input Interface Spec**	Velsanet TSG requires: 8-ch parallel digital baseband input, channel-to-slot alignment per sector. RF processing (PHY, MAC, beam-forming) is the responsibility of the 6G RU manufacturer.	Interface boundary: digital baseband output of 6G RU to TSG input	1	

	Time-Sensitive Gearbox (TSG)				
3	**Fixed-Delay Wiring Fabric**	FPGA / custom ASIC, 8 hard-wired parallel paths, no scheduler, no FIFO	Propagation delay< 2 ns, ±50 ps channel match	1	
4	**Slot Alignment Circuit**	8-lane delay line, hardware-matched across all channels	Jitter < 50 ps end-to-end	1	
	MOCT Physical Interface				
5	**Coherent Optical Engine**	Wireless-to-optical mapper, sector-to-core hard-wired	Core #2–#47 (46 data cores), 3.6x capacity reserve	1	
6	**Slave Laser (OIL)**	Injection-lockable laser cavity, coupled to Core #48	Lock bandwidth > 1 GHz, jitter < 1 fs post-lock	1	
7	**Polymer Optical Core Layer**	48-core polymer waveguide array, 8 fixed channels per core	Core #1=control, Core #48=clock, #2–#47=data	1	
8	**Mechanical Contact Layer**	Static micro-contacts, micron-level alignment, no moving parts	Vibration-resistant, zero operational power	1	
9	**MEMS Alignment Layer**	Silicon photonics matrix+ static MEMS, lithographic precision	Temp-invariant, -20°C to +60°C	1	
10	**Pre-attached Ribbon Cable (RU)**	48-core single-mode ribbon, factory-fused, no connectors	Length 7 m, permanently bonded	1	
	Mechanical & Power				
11	**Weatherproof Enclosure**	IP67-rated outdoor housing, pole-top mount	Operating range -20°C to +60°C	1	
12	**Pole Mounting Bracket**	Clamp + tilt-adjust bracket for utility pole top	Pole diameter 80–150 mm	1	
13	**Power Supply Unit**	DC input or PoE++, surge protection, no active cooling	Power draw < 15 W per RU	1	

6.2 Pole-Site Assembly BOM (per pole)

#	Item	Specification	Segment / Role	Qty	
1	**6G RU (complete unit)**	Per 6.1 BOM above, pole-top installation	Wireless entrypoint — Seg A origin	1–3 / pole	
2	**H6 Node**	C6 Hexahedron, 6-face, autonomous, installed at +2 m	RAN mesh anchor	1 / pole	
3	**MOCT Ribbon — H6 Face 1**	48-core, 5 m, factory pre-attached to H6	Seg A — fused with RU cable	1 / pole	

4	**MOCT Ribbon — H6 Face 2**	144-core (12x12 stack), 5 m, factory pre-attached	Seg C — H6 to O8 uplink	1 / pole	
5	**MOCT Ribbon — H6 Face 3**	48-core, 5 m, factory pre-attached	Seg B — H6 to adjacent H6 mesh	1 / pole	
6	**MOCT Ribbon — H6 Face 4**	48-core, 5 m, factory pre-attached	Seg B — H6 to adjacent H6 mesh	1 / pole	
7	**MOCT Ribbon — H6 Face 5**	24-core, 5 m, factory pre-attached	T4 downlink	1 / pole	
8	**MOCT Ribbon — H6 Face 6**	48-core, 5 m, factory pre-attached	Reserved / expansion	1 / pole	
9	**Ribbon Fusion Splice Kit**	Full-ribbon simultaneous fusion, field-grade	RU cable + H6 Face-1 splice (Seg A)	1 / pole	
10	**Underground Conduit Section**	144-core armored ribbon, H6 to building wall entry	Seg C buried run	per m	
11	**Pole Ground Enclosure / Shroud**	H6 protective housing, IP67, tamper-resistant	H6 installation enclosure at +2 m	1 / pole	

Note: All MOCT ribbon cables are factory pre-attached and non-detachable. Field installation involves only ribbon fusion splicing at designated splice points; no pluggable connectors exist in any Velsanet node interface. Quantities marked per m are determined by site survey at deployment time.

White Paper #23 — Velsanet Architecture Group

Core Concept	Structure-Native physical path direct mapping, no software switching
Reference Docs	WP #02, #03, #22 · Velsanet Architecture Compendium v1.0 (2026)